UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/695,756	10/24/2000	Thomas W. Voshell	500080.02	2589

27076	7590	03/11/2004

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EXAMINER
LAMARRE, GUY J

ART UNIT	PAPER NUMBER
2133	2

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _1/13/04_ .

2a)☐ This action is **FINAL**.　　　　2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under _Ex parte Quayle_, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _41-67_ is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _41-67_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

　　If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All b)☐ Some * c)☐ None of:

　　　　1.☐ Certified copies of the priority documents have been received.

　　　　2.☐ Certified copies of the priority documents have been received in Application No. _____ .

　　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

　　a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5)☐ Notice of Informal Patent Application (PTO-152)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6)☐ Other: _____ .

DETAILED ACTION

Response to Amendment

1.   This office action is in response to Applicants' amendment, filed on *13 January 2004*.

1.1   **Claims 41-67** remain pending.

1.2   The prior art rejections of record <u>are withdrawn</u> in response to Applicants' amendment, filed on *13 January 2004.*

Response to Arguments

2.   Applicants' arguments, filed on *13 January 2004*, have been fully considered and are persuasive only to the extent that **Akamatsu et al.** does not specifically detail addressing compression means as claimed. However, upon further consideration/search, a new ground(s) of rejection is made as follows. **Park et al.** 'Address compression through base register caching' teaches such addressing compression means for a VLSI chip comprising memory and CPU in Fig. 1 as seen below, wherein addresses are compressed to reduce storage requirements by 60% without degrading system performance in Abstract and pages 193-199.
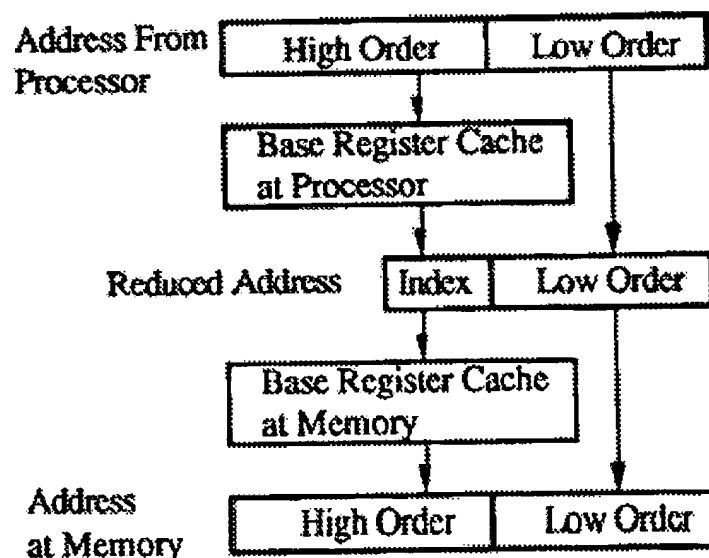
Address From Processor — High Order | Low Order

Base Register Cache at Processor

Reduced Address — Index | Low Order

Base Register Cache at Memory

Address at Memory — High Order | Low Order

Figure 1: Base Register Caching

Claim Rejections - 35 USC ' 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.0   Claims **41-43, 45-48** and **54-64** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Akamatsu et al.** (US Patent No. 6,134,681) in view of **Hancu et al.** "A concurrent test architecture for massively parallel computers and its error detection capability; IEEE Transactions on Parallel and Distributed Systems," and **Park et al.** 'Address compression through base register caching, 'IEEE; 27-29 Nov. 1990; On page(s): 193 – 199.

As per Claims 41, 45, 54-55, 59, 64, Akamatsu et al. substantially discloses the procedure for the claimed method of accessing a memory via test instructions or commands, means to initiate test mode, comprising: comparing memory addresses for a fault memory analysis (access/test) by performing substitute address allocation (mapping or remapping) and provides compression means wherein decompressed addresses are used in memory access or transfer in col. 2 lines 35-50. {See **Akamatsu et al.,** Id., Figs. 1-17 and related description, e.g., col. 7 line 4 et seq., wherein means is provided for remapping defective memory address with spare memory address}. **Not specifically described** in detail in **Akamatsu et al.** is the step whereby compressing is effected on addresses as a means for reducing failure storage hardware.

However such memory address compressing approach is well known in memory testing. For example, **Hancu** and **Park et al.** in an analogous art, disclose algorithms wherein such techniques are described including error detection routine based on comparison of routing or address signatures in compressed format. {See **Hancu et al.,** Id., Figs. 4-14, Tables 1-4 and associated description on pages 1170-1183, including intermediate queuing or buffering or memory means on page 1172 col. 2 para. 2. Data transfer performing equivalent functionality as data storage. Also refer to **Park et al.** wherein techniques, for memory address compressing in

VLSI ICs on page 196 col. 2 para. 2 and Fig. 1, comprises compaction means of high order address portion and decompressed means for lower order address portion for circuit reduction.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Akamatsu et al.** by including therein address compression means as taught by **Hancu** and **Park et al.**, because such modification would provide the procedure disclosed in **Akamatsu et al.** with a technique whereby *"hardware is optimized so as to limit the size of the processing units for maximum integration and minimum cost."* {See **Hancu et al.**, Id., page 1171 col. 2 para. 6 et seq.; also refer to **Park et al.**, Id., page 195 col. 2 para. 3 et seq.}

As per **Claim 42, 46-47** and **56, Hancu et al.** discloses the procedure for decompressing addresses for comparison so as to ease localization of failure on page 1172 col. 2 paras. 3-5. Also see **Park et al.** at page 196 col. 2 para. 2 and Fig. 1.

As per **Claims 43** and **48, Hancu et al.** discloses the procedure for decompressing addresses for comparison so as to ease localization of failure on page 1172 col. 2 paras. 3-5. Also see **Park et al.** at page 196 col. 2 para. 2 and Fig. 1.

As per **Claim 58, Hancu et al.** discloses the procedure for initiating test command at powering up the memory on page 1169 col. 2 paras. 1-2, wherein errors are detected on-line or concurrently with execution of parallel program. Also see **Park et al.** at page 196 col. 2 para. 2 and Fig. 1.

As per **Claim 60, Hancu et al.** discloses the procedure for intermediate queuing or buffering or memory or storage means on page 1172 col. 2 para. 2. Also see **Park et al.** at page 196 col. 2 para. 2 and Fig. 1.

As per Claim 61, Hancu et al. discloses the procedure for testing or detecting faults

prior to forwarding data to intermediate location or accepting memory requests on page 1172 col.

2 para. 2, page 1176 col. 1 Section B. Also see Park et al. at page 196 col. 2 para. 2 and Fig. 1.

As per Claim 62, Hancu et al. discloses the procedure for compressing addresses prior

to storage or transfer, e.g., on page 1169 col. 2 penultimate para., or page 1172 col. 2 para. 2,

viz., "both the routing and control streams are signatured (compressed)." Also see Park et al. at

page 196 col. 2 para. 2 and Fig. 1.

As per Claims 63 and 57, Hancu et al. discloses the procedure for compressing

addresses wherein all compressed addresses have unique signature to thereby ease localization of

failure on page 1172 col. 2 paras. 3-5 subsequent to decompressing compressed addresses for

comparison. Also see Park et al. at page 196 col. 2 para. 2 and Fig. 1.

3.1   Claims 44, 49-53, 65-67 is/are rejected under 35 U.S.C. 103(a) as being unpatentable
over Akamatsu et al. (US Patent No. 6,134,681) in view of Hancu et al. and Park et al.
'Address compression through base register caching.' in further view of Meaden (US Patent No.
4,642,793; March 19, 1984).

As per Claims 44, 49-53, 65-67, Akamatsu/Park/Hancu substantially disclose the

procedure for the claimed method of claim 42. Not specifically described in detail in Akamatsu

et al. or Hancu or Park is the step whereby calculating a value from the memory address

comprises dividing the value represented by the memory address by a prime number or use of

hashing code or function.

However such memory address generation approach is well known in data compression.

For example, Meaden, in an analogous art, discloses algorithms in "Many-to-one mapping hash

address generator" wherein such techniques are described. {See Meaden, Id., Abstract.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the

invention was made to modify the procedure of Akamatsu/Park/Hancu by including therein

address generation means via prime numbers or hashing code or function as taught by **Meaden,**

because such modification would provide the procedure disclosed in **Akamatsu/Park/Hancu**

with a technique whereby *"The indicator R is also applied to the address input of a random*

access memory 37 having four locations, each of which contains <u>a prime number</u> in the range

3-251. The contents of the addressed location of the memory 37 supply the hashing key K for

the <u>hash coding circuit 30</u>. " {See **Meaden, col.** 3 line 27 et seq.}

3.1.1 **Claims 44, 49-53, 65-67** is/are rejected under 35 U.S.C. 103(a) as being unpatentable over **Akamatsu et al.** (US Patent No. 6,134,681) in view of **Hancu et al.** and **Park et al.** 'Address compression through base register caching.' in further view of **Matsuda** (US Patent No. 5,659,737; August 1, 1995).

As per Claims 44, 49-53, 65-67, Akamatsu/Park/Hancu substantially disclose the

procedure for the claimed method of claim 42. **Not specifically described** in detail in **Akamatsu**

et al. or **Hancu** or **Park** is the step whereby calculating a value from the memory address

comprises dividing the value represented by the memory address by a prime number or use of

hashing code or function.

However such memory address generation approach is well known in data compression.

For example, **Matsuda,** in an analogous art, discloses algorithms in *"Methods and apparatus for*

data compression that preserves order by using failure greater than and failure less than tokens"

wherein such techniques are described. {See **Matsuda,** Id., Abstract.} **Therefore,** it would have

been obvious to a person having ordinary skill in the art at the time the invention was made to

modify the procedure of **Akamatsu/Park/Hancu** by including therein address generation means

via prime numbers or hashing code or function as taught by **Matsuda,** because such modification

would provide the procedure disclosed in **Akamatsu et al.** and **Hancu** with a technique whereby

"FIG. 2 conceptually illustrates a mapping of predictive substrings, PS, from the character

string 105 into the hash table 110. As shown by the lines and arrows in FIG. 2, for each

predictive substring (PS), a hash index, specified by a hash function, maps the (PS) into an

entry in the hash table 110. For the example shown in FIG. 2, the predictive substring

(PS.sub.i) containing the characters "ABC" maps into a hash table entry for storage of the

successive character "D." Similarly, for the additional substrings (PS.sub.i+1, PS.sub.i+2, and

PS.sub.i+3), each predictive substring maps into the hash table 110. These examples assume

that the natural language indications properly predict the successive character. The order of

the characters in hash table 110 is merely exemplary, and the actual storage of characters is

based on the hash function. Any hash based predictive function may be used in conjunction

with the present invention to map the predictive substrings into the entries of hash table 110.

In one embodiment, a remainder of division technique is used. The remainder of division

technique is defined by the function   h(key)=key MOD M where the devisor M determines

the effective size of the hash table and is a prime number. The key is defined as the predictive

substring. The remainder of division hash function works well when the block size is relatively

small, such as when the block size is 3. " {See **Matsuda, col. 2** line 56 et seq.}

3.1.2   Claims 44, 49-53, 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Akamatsu et al.** (US Patent No. 6,134,681) in view of **Hancu et al.** and **Park et al.** 'Address compression through base register caching.' in further view of **NN8806199** (Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory; IBM Technical Disclosure Bulletin, June 1988, US; VOLUME NUMBER: 31, PAGE NUMBER: 199 – 202, hereinafter **IBM Tech**).

As per **Claims 44, 49-53, 65-67, Akamatsu/Park/Hancu** substantially disclose the

procedure for the claimed method of claim 42. **Not specifically described** in detail in **Akamatsu**

et al. or **Hancu** or **Park** is the step whereby calculating a value from the memory address

comprises dividing the value represented by the memory address by a prime number or use of

hashing code or function.

However such memory address generation approach is well known in data compression. For example, **IBM Tech,** in an analogous art, discloses algorithms wherein such techniques are described. {See **IBM Tech,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Akamatsu/Park/Hancu** by including therein address generation means via prime numbers or hashing code or function as taught by **IBM Tech,** because such modification would provide the procedure disclosed in **Akamatsu/Park/Hancu** with a technique whereby *"many subsets of the chained blocks are arranged so that they are contained in the same memory segment and their relative order is maintained. The standard index table contains an entry for each block comprising the array. The modified indexing table contains an entry for each memory segment that contains a logically contiguous subset of the chained blocks. In addition, each table entry contains a count of the number of blocks mapped by the entry, that is, the number of blocks contained within the memory segment indicated by the entry. If many blocks fit within a single memory segment, each entry in the indexing table may indicate several blocks instead of just one. This table is more compact than a general index that pointed to each block and therefore will cause less page and cache faults, in addition to occupying less memory. The modified indexing structure is shown in Fig. 3. The same set of blocks as used in Fig. 2 are modified into a smaller indexing table."* {See **IBM Tech,** last 10 lines.}

Conclusion

4.   Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to:

(703) 872-9306 for formal communications intended for entry,

(703) 746-5463 for informal or draft communications, please label "PROPOSED" or "DRAFT".

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington,

VA, <u>Fourth Floor</u> (Receptionist).

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-

0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre, P.E.
Patent Examiner
6 March 2004